WHAT IS CLAIMED IS:

1. An output stage comprising:

a p-channel inverter device coupled to a first supply voltage;

a p-channel stacked device coupled between the p-channel inverter and a pad;

an n-channel stacked device coupled to the pad; and

an n-channel inverter device coupled between the n-channel stacked device and a second supply,

wherein a gate of the p-channel stacked device receives a first bias voltage and a gate of the n-channel stacked device receives a second bias voltage, and the first bias voltage and the second bias voltage vary depending on a voltage difference between the first supply voltage and the second supply voltage.

2. The output stage of claim 1 further comprising:

a first voltage translator coupled to a gate of the p-channel inverter device, wherein the first voltage translator translates a signal in a first voltage range to a second voltage range, the second voltage range defined by the first supply voltage and the second supply voltage.

3. The output stage of claim 2 further comprising:

a second voltage translator coupled to a gate of the n-channel inverter device, wherein the second voltage translator translates a signal in the first voltage range to the second voltage range.

4. The output stage of claim 3 wherein the second supply voltage is ground.

5. The output stage of claim 1 wherein the output stage is tri-stated by setting the first bias voltage approximately equal to the first supply voltage and the second bias voltage approximately equal to the second supply voltage.

6. The output stage of claim 5 wherein the n-channel stacked device receives the first bias voltage at its gate, and the p-channel stacked device receives the second bias voltage at its gate.

7. The output stage of claim 5 wherein when the voltage difference between the first supply voltage and the second supply voltage is approximately equal to the sum of the drain-to-source breakdown voltages for the p-channel and n-channel inverter devices, the first bias voltage and the second bias voltage are approximately equal and near the mid-point between the first supply voltage and the second supply voltage.

8. The output stage of claim 7 wherein the bulk of the p-channel stacked device is coupled to a body bias circuit, and

wherein the body bias circuit generates a voltage that tracks the higher voltage between the first supply voltage and a received voltage.

9. An integrated circuit comprising:

an input stage coupled to a pad;

an output stage coupled to the pad; and

a bias circuit coupled to the pad

wherein the output stage comprises a first p-channel device coupled to the pad, the first p-channel device comprising a bulk, a drain, a gate, and a source, and the bulk is connected to the bias circuit, and

wherein the gate of the first p-channel device receives a first bias voltage, and the first bias voltage is selected based on a supply voltage received by the output stage.

10. The integrated circuit of claim 9 wherein the output stage further comprises:

a second p-channel device coupled to receive the supply voltage and further coupled to the first p-channel device.

11. The integrated circuit of claim 10 wherein the output stage further comprises:

a first n-channel device coupled to the first p-channel device, the first n-channel device comprising a gate,

wherein the gate of the first n-channel device receives a second bias voltage, and the second bias voltage is selected based on a supply voltage received by the output stage.

12. The integrated circuit of claim 10 further comprising:

a first voltage translator coupled to a gate of the first p-channel device, wherein the first voltage translator translates a signal in a first voltage range to a second voltage range, the second voltage range defined by the first supply voltage and a second supply voltage, wherein the second supply voltage is ground.

13. An integrated circuit comprising:

an input stage coupled to a pad;

an output stage coupled to the pad and receiving a first power supply; and

a bias circuit coupled to the pad

wherein the output stage comprises a first p-channel device coupled to the pad, the first p-channel device comprising a bulk, a drain, a gate, and a source, and the bulk is connected to the bias circuit, and

wherein the bias circuit comprises a first device and a second device coupled in series between the pad and the bulk of the first p-channel device, the first device biased to protect the second device from voltages on the pad.

14. The integrated circuit of claim 13 wherein a gate of the second device is coupled to the first power supply.

15. The integrated circuit of claim 14 wherein a gate of the first device is coupled to a bias voltage, the bias voltage set to protect the first device from voltages on the pad.

16. The integrated circuit of claim 13 wherein the first device and the second device are p-channel devices.

17. The integrated circuit of claim 13 wherein the output stage further comprises:

a second p-channel device coupled to receive the first supply voltage and further coupled to the first p-channel device, wherein the bulk of the first p-channel device is coupled to the bulk of the second p-channel device.

18. The integrated circuit of claim 17 further comprising:

a first voltage translator coupled to a gate of the first p-channel device, wherein the first voltage translator translates a signal in a first voltage range to a second voltage range, the second voltage range defined by the first supply voltage and a second supply voltage, wherein the second supply voltage is ground.

19. The integrated circuit of claim 13 wherein the first p-channel device receives a bias voltage at its gate, and the bias voltage is determined by the first supply voltage.

20. The integrated circuit of claim 19, wherein the integrated circuit is a programmable logic device.